

A COUPLED INDUCTOR BASED CASCADED HIGH STEP UP DC-DC CONVERTER WITH LOW DUTY CYCLE

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Abstract

Devices such as fuel cells, photovoltaic cells and wind turbines convert the energy of sustainable energy resources into electricity but with very low output voltages. When used for distributed generation system or grid connected operation, as a front end converter, a high gain dc converter becomes an essential requirement for all these sources. This article presents high gain cascaded dc-dc converter based on coupled inductor for renewable energy sources based applications. It uses a single switch and also includes integrated voltage multiplier cell to achieve high gain with minimum losses. In addition, the converter presented in this paper attains high voltage conversion ratio at low operating duty ratio with reduced voltage stress across active switch and small turns ratio. The couple inductor's leakage energy is recycled. Additionally, small voltage stresses across diodes facilitates faster reverse recovery. These features decrease the conduction losses as well as cost and also increase conversion efficiency. The analysis of the proposed converter's steady-state operation is presented in detail as well as the voltage conversion ratio is derived. PSpice simulation software is used for validating the theoretical analysis along with performance of the proposed converter.

Keywords – DC-DC converter · Sustainable energy · Coupled inductor · High voltage gain · Low voltage stress

1 – Introduction

In the last few decades the global electricity demand has been increasing due to increase in technology applications in day to day life. At present, most of the global electricity demand has been fulfilled by fossil fuels such as oil, coal and natural gas. As of 2019, fossil fuels have 62.76% share (coal – 36.38%, natural gas – 23.32% and oil – 3.06%), in total electricity generation in the world [1]. Burning of fossil fuels for generation of electricity is the largest contributor to the global air pollution. Air pollution has become significant threat to both environment as well as human health worldwide. Fossil fuel air pollution alone is responsible for more than 8 million worldwide premature deaths every year implying 1 of every 5 deaths [2]. Hence an urgent action is required to accelerate the transition to clean renewable energy sources. This includes solar and wind energy for generation of electrical power. Hydrogen is a versatile energy carrier which is considered as another promising alternative to fossil fuel. Fuel cells (FC) are electrochemical devices that can be utilized for converting Hydrogen's chemical energy directly to electrical energy. It does not require any intermediate stage. Hydrogen and FC technologies are considered as an excellent solution for clean energy generation as FC produces only water and heat as by-products.

The output voltage produced by FC stacks, wind turbines and photovoltaic (PV) arrays are usually low and unstable. For a renewable energy-based distributed generation (DG) system or grid connected operation, a power conditioning system (PCS) is an essential requirement. This PCS typically consists of a dc to dc converter to step up lower voltages generated by renewable sources including FC stacks, wind turbines and PV arrays to a higher level followed by a dc to ac inverter, for achieving grid voltage of

220-V. The front end dc to dc converter must convert lower voltage levels (20 to 48V) to higher voltage levels (380 – 400V).

The uses of 380V dc distribution systems for data centers and commercial buildings are considerably increasing. In many utilities, dc distribution systems provide more efficient, more reliable service over ac distribution systems. Moreover, they incur less up-front capital cost and occupy less floor space [3]. Thus the need of high gain dc–dc converters for a variety of applications is increasing. In the last couple of decades, researchers have proposed numerous topologies using different boosting techniques for obtaining high voltage gain working on various features.

Adding switch capacitor (SC) cells to a conventional boost converter (CBC) results in a significant increase in voltage gain [4 - 7]. The voltage gain of SC converters depends on number of capacitors and their arrangement in the converter. In this technique, higher gain is achieved from capacitive energy transfer by charging the switched capacitors in parallel and discharging in series. However, switching capacitors cause a large surge current at the active switch resulting in large losses. Hence, the SC converters are useful in very low power applications. Some SC converters follow the concept of charge pumping to enhance the voltage conversion ratio where energy is transferred from one capacitor to another capacitor [8]. By incorporating the switch inductor cell into CBC, a large voltage gain may be attained [9]. Some high-order switched inductor converters are presented in [10 - 11] to obtain higher voltage gains. A combination of switched inductor and switched capacitors is another alternative for obtaining a high voltage gain [12].

Many topologies are presented by researchers in the literature that combine the features of VMC (voltage multiplier cells) and CBC to obtain high voltage conversion ratio. VMCs increase the gain by adding a small number of extra components, typically a set of different configurations of capacitors and diodes [13 - 14]. Use of inductors in VMCs helps the circuit to achieve higher voltage-boosting ratio [15].

Coupled inductors may be used effectively in the boost converters to increase voltage conversion ratio along with decrease in switch voltage stress [16]. This technique also efficiently handles the output diode's reverse-recovery issue. It has become one of the most widely used techniques in high gain converters. In such converters, high voltage conversion ratio may be obtained at lower duty ratio depending upon the selection of its turn-ratio.

Multiple boost converters can be cascaded together to improve voltage gain. In [17], a converter comprising of two CBCs cascaded together is investigated. In such a cascaded boost converter, the voltage conversion ratio is calculated as a product of voltage conversion ratios of all stages. However, this method suffers from significant drawbacks of having a large number of components, reduced efficiency and less system reliability. The multistage cascaded boost converter's switches may be merged into one switch to simplify circuit complexity [18]. This converter is called as quadratic boost converter (QBC). The major drawback of QBC is very large voltage stresses on both the switch as well as output diode.

To further increase the voltage conversion ratio with decreased voltage stresses across switch, literature suggested integration of Capacitor Inductor Diode (CLD) cell [19], active clamp circuit [20], VMC [21], voltage doubler voltage lift circuit [22] and coupled inductor with QBC.

Based on this literature review, this paper presents a high gain cascaded boost converter based on the coupled inductor and an integrated voltage multiplier cell. The salient features of the proposed converter include high voltage conversion ratio, single switch, low duty cycle, low switch voltage stress and higher conversion efficiency. Thus integration of the clamp circuit with the coupled inductor's secondary and slightly different arrangements of components like diodes and capacitors in the VMC has given better results.

2 – Operating principle

The system configuration of the proposed high step up converter topology is illustrated in Fig. 1(a). Two boost converters are cascaded to form this single switch converter. The first stage is conventional boost converter comprising of Inductor L_1 , diodes D_1 , D_2 and capacitor C_1 . The switch S is common for both the stages. The second stage is coupled inductor based boost converter with integrated VMC. Diode D_3 and C_2 act as a clamp circuit but at the same time C_2 along with D_4 and the coupled inductor's secondary winding also help VMC to further enhance the voltage conversion ratio. In this converter, charging of capacitors C_3 and C_4 takes place in parallel while discharging in series to obtain higher output voltage. The capacitor C_4 is charged by coupled inductor's secondary whereas capacitor C_3 is charged by the series combination of capacitor C_2 and coupled inductor's secondary.

The proposed converter's equivalent circuit is illustrated in Fig. 1(b) in which the coupled inductor is represented as a combination of an ideal transformer, a magnetising inductance L_m and a leakage inductance L_k .

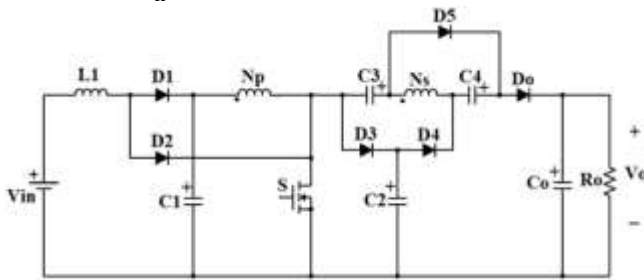


Fig. 1(a): Proposed converter

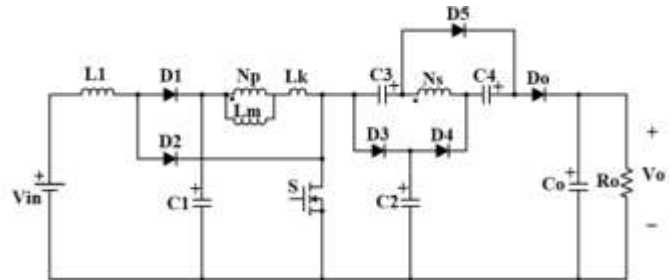


Fig. 1(b): Equivalent circuit

Note that, in this discussion, currents through and voltages across various components are represented as follows: $L_1 : i_{L1}, v_{L1}$, $L_m : i_{Lm}, v_{Lm}$, $L_k : i_{Lk}, v_{Lk}$, $D_1 : i_{D1}, v_{D1}$, $D_2 : i_{D2}, v_{D2}$, $D_3 : i_{D3}, v_{D3}$, $D_4 : i_{D4}, v_{D4}$, $D_5 : i_{D5}, v_{D5}$, $D_0 : i_{D0}, v_{D0}$, $C_1 : i_{C1}, v_{C1}$, $C_2 : i_{C2}, v_{C2}$, $C_3 : i_{C3}, v_{C3}$, $C_4 : i_{C4}, v_{C4}$, $C_0 : i_{C0}, v_{C0}$, coupled inductor's primary and secondary windings as i_1, i_2 and v_{Np}, v_{Ns} respectively. The V_{DS} and V_{GS} are drain-to-source and gate-to-source voltages of MOSFET which is used as an active switch.

Figure 2 demonstrates proposed converter's some typical waveforms in steady state condition for one switching cycle in four operating modes in Continuous Conduction Mode (CCM). The operating principle in each mode is explained below. Figure 3 illustrates the equivalent circuits for all modes.

Mode 1 [t_0, t_1]:

The switch S is turned ON at time t_0 . During this mode, diodes D_2 , D_4 along with D_5 become forward biased whereas diodes D_1 , D_3 as well as D_0 become reverse biased. Figure 3(a) depicts the current flow path. The inductor L_1 is subjected to the input voltage V_{in} results in increase in inductor current i_{L1} in a linear fashion. The voltage V_{C1} appears across the magnetizing inductance L_m and leakage inductance L_k that results in increase in i_{Lm} and i_{Lk} . The portion of the energy stored in capacitor C_1 is delivered to capacitor C_3 and C_4 via the coupled inductor's secondary winding. Simultaneously, energy stored in capacitor C_2 is also transferred to C_3 via D_4 , secondary winding and switch S . Increase in capacitor voltages V_{C3} and V_{C4} cause capacitor currents i_{C3} and i_{C4} to reduce linearly. At time t_1 , the capacitor currents i_{C3} and i_{C4} become zero which turns off diodes D_4 and D_5 . This forces currents i_{C2} and i_2 to zero. The output capacitor C_0 supplies the load current. This mode ends at time t_1 .

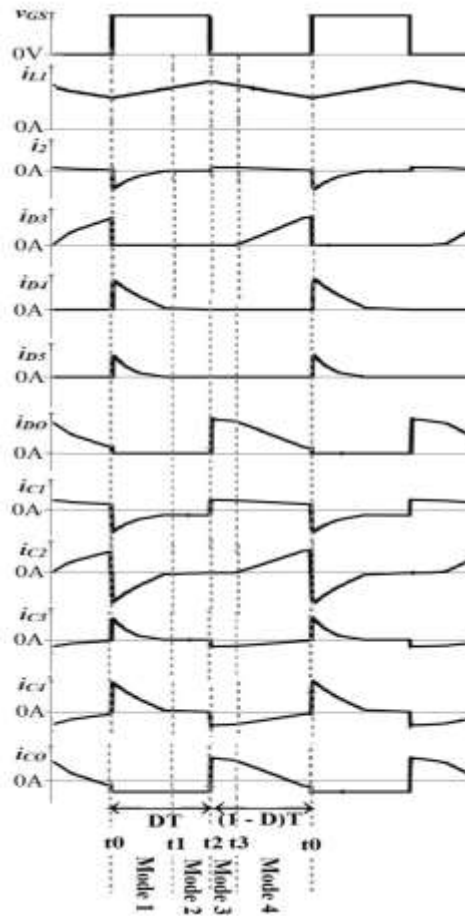


Fig. 2: Key waveforms of the proposed converter

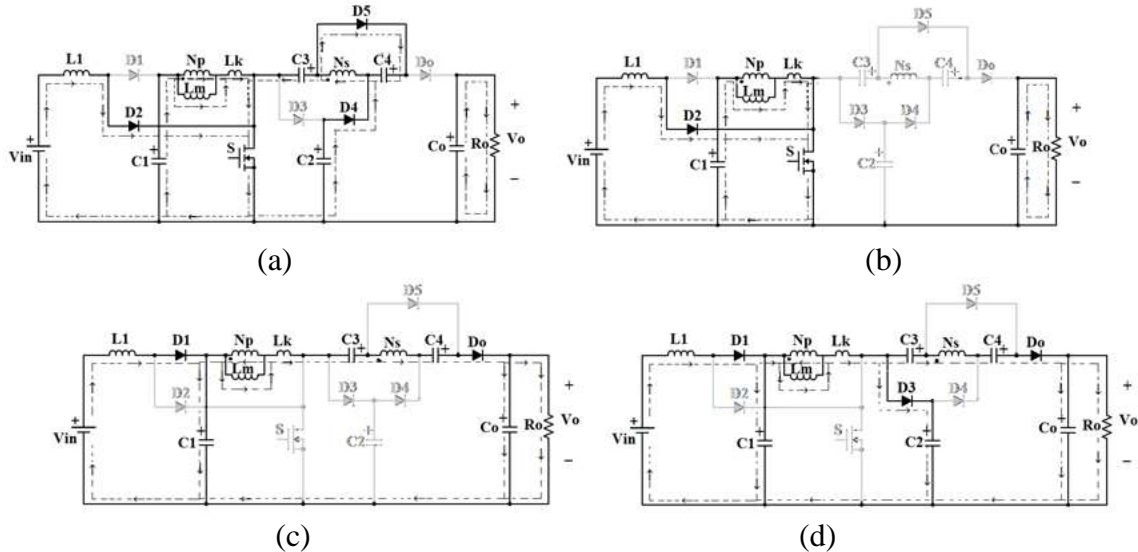


Fig. 3 Operating Modes (a) Mode 1, (b) Mode 2, (c) Mode 3, (d) Mode 4

Mode 2 [t_1, t_2]:

The switch S along with diode D_2 are ON whereas diodes D_1, D_3, D_4, D_5 along with D_o become reverse biased. Figure 3(b) illustrates the current flowing path. The currents i_{L1}, i_{Lm} and i_{Lk} continue to increase

linearly. The capacitor currents i_{C2} , i_{C3} , i_{C4} and secondary winding current i_2 remain zero during this mode. Input source V_{in} and capacitor C_1 continue to deliver energy to inductors L_1 and L_m respectively. The load energy is continued to be delivered by the output capacitor C_O . At time t_2 , switch S is turned OFF and this mode ends.

Mode 3 [t_2 , t_3]:

At time t_2 the switch S is turned OFF. Diodes D_1 and D_O become forward biased, diodes D_2 , D_3 , D_4 along with D_5 become reverse biased. Figure 3(c) depicts the current flowing path. The voltage ($V_{in} - V_{C1}$) appears across the inductor L_1 . This voltage is negative as $V_{C1} > V_{in}$ resulting in linear decrease in inductor current i_{L1} . During this interval, the leakage current i_{Lk} initially decreases rapidly and then linearly. The part of the energy from input source V_{in} and inductor L_1 is released to capacitor C_1 . During this mode, capacitor currents i_{C1} , i_{C3} , i_{C4} , i_{C_O} and secondary current i_2 initially change rapidly in opposite direction and then decrease linearly. At time t_3 the reducing secondary current i_2 equals i_{Lk} . After that the difference of currents $i_{Lk} - i_2$ turns ON diode D_3 and supplies energy to capacitor C_2 . The series voltages of input source, inductor L_1 , primary winding, C_3 , secondary winding and C_4 charge capacitor C_O and supplies output load R_O . This mode ends at time t_3 .

Mode 4 [t_3 , t_4]:

During this mode switch S remains OFF, diodes D_2 , D_4 , D_5 are blocked while diodes D_1 , D_3 , D_O conduct. Figure 3(d) illustrates the current flowing path. The series voltages of input source, inductor L_1 , primary winding, C_3 , secondary winding and C_4 continue to charge C_O and supply the output load R_O . Meanwhile capacitor C_1 gets energy from V_{in} and inductor L_1 through D_1 whereas C_2 gets energy from V_{in} , inductors L_1 and L_m through D_3 . At time t_0 , switch S is turned ON and the switching cycle repeats.

3 - Steady state analysis

Following assumptions are considered to simplify steady state analysis.

- All components are ideal except the coupled inductor where its leakage inductance is taken under consideration.
- All capacitance values are sufficiently large to provide constant capacitor voltages.
- The inductor currents i_{L1} and i_{Lm} are continuous (always positive).
- The coupled inductor's turns ratio $n = N_s/N_p$.

Voltage gain

Apply KVL to Fig. 3(a) during switch ON condition to get following two equations

$$V_{L1(ON)} = V_{in} \quad (1)$$

$$V_{Lm(ON)} = V_{C1} \quad (2)$$

$$V_{C4} = V_{N_s(ON)} \quad (3)$$

$$V_{C2} + V_{N_s(ON)} - V_{C3} = 0 \quad (4)$$

During switch ON state, the secondary winding voltage may be given as

$$V_{N_s(ON)} = n V_{Lm(ON)} \quad (5)$$

Substituting (2) and (5) in (3), V_{C4} can be written as

$$V_{C4} = n V_{C1} \quad (6)$$

Similarly substituting (2) and (5) in (4), we get

$$V_{C2} + n V_{C1} - V_{C3} = 0 \quad (7)$$

By applying KVL to Fig. 3(d) during switch S OFF state gives

$$V_{L1(OFF)} = V_{in} - V_{C1} \quad (8)$$

$$V_{Lm(OFF)} = V_{C1} - V_{C2} \quad (9)$$

$$V_{C2} + V_{C3} - n V_{N_s(OFF)} + V_{C4} - V_O = 0 \quad (10)$$

The secondary winding voltage during switch OFF state can be expressed as

$$V_{Ns(OFF)} = n V_{Lm(OFF)} \quad (11)$$

Substituting (9) and (11) in (10), we get

$$V_o = V_{C2} + V_{C3} - n(V_{C1} - V_{C2}) + V_{C4} \quad (12)$$

Apply volt-second balance principle across L_1 gives

$$V_{L1(ON)}t_{ON} + V_{L1(OFF)}t_{OFF} = 0 \quad (13)$$

Substituting $t_{ON} = DT$ and $t_{OFF} = (1 - D)T$ into (13) yields

$$V_{L1(ON)}DT + V_{L1(OFF)}(1 - D)T = 0 \quad (14)$$

Substituting (1) and (8) in (14) and solving for V_{C1} gives

$$V_{C1} = \frac{1}{1-D} V_{in} \quad (15)$$

Apply volt-second balance principle across L_m and solve for V_{C2}

$$V_{C2} = \frac{1}{1-D} V_{C1} \quad (16)$$

The voltage V_{C3} can be derived by substituting (15) and (16) in (7)

$$V_{C3} = \frac{1+n-nD}{1-D} V_{C1} \quad (17)$$

Using equations (6), (12), (15), (16) and (17), the output voltage V_o may be computed as follows.

$$V_o = \frac{2+2n-nD}{(1-D)^2} V_{in} \quad (18)$$

Thus, the voltage conversion ratio is represented below.

$$M = \frac{V_o}{V_{in}} = \frac{2+2n-nD}{(1-D)^2} V_{in} \quad (19)$$

Figure 4 shows a plot of voltage conversion ratio against duty ratio for various values of coupled inductor's turns ratio for the proposed converter. It demonstrates that as the turns ratio increases, so does the voltage conversion ratio.

Voltage stresses

Figure 3 (d) can be referred to find out the switch voltage stress.

$$V_{S(OFF)} = V_{C2} = \frac{1}{2+2n-nD} V_o \quad (20)$$

The voltage stresses across diodes are derived and represented below.

$$V_{D1(OFF)} = V_{C1} = \frac{1-D}{2+2n-nD} V_o \quad (21)$$

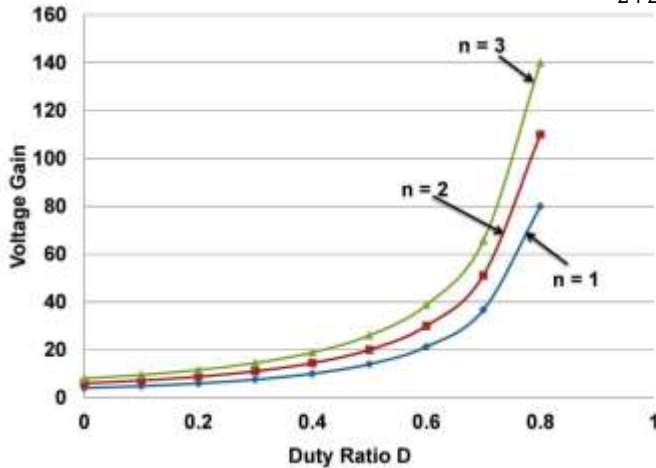


Fig. 4: Voltage gain Vs Duty ratio

$$V_{D2(OFF)} = V_{D3(OFF)} = V_{C2} = \frac{1}{2+2n-nD} V_o \quad (22)$$

$$V_{D4(OFF)} = V_o - V_{C2} - V_{C4} = \frac{1+n}{2+2n-nD} V_o \quad (23)$$

$$V_{D5(OFF)} = V_{Ns(OFF)} - V_{C4} = \frac{n}{2+2n-nD} V_o \quad (24)$$

$$V_{DO(OFF)} = V_o - V_{C3} = \frac{1+n}{2+2n-nD} V_o \quad (25)$$

The voltage stress across D_o equals the difference between the output voltage and voltage of capacitor C_3 . Thus, the voltage stress across output diode is always smaller than the converter output voltage.

Performance comparison with other topologies

Table 1 compares the proposed converter’s major parameters to those of two recently published converters in order to demonstrate its performance. For fair comparison, converters presented in [23] and [24] are chosen because the voltage boosting technique used (cascading, coupled inductor and VMC) and choice of components (viz. single switch, one inductor, one coupled inductor, six diodes and five capacitors) match exactly with that of the proposed converter. However, results of converter presented in this paper are better because of the modified configuration of the same.

Table 1 Performance comparison with other topologies

Reference	Components# S/L/CL/D/C	Voltage gain	Voltage stress on switch	Voltage stress on output diode
[23]	1/1/1/6/5	$\frac{n(3D + 2) + (2 - D)}{2(1 - D)^2}$	$\frac{(2 + D(n - 1))V_o}{n(3D + 2) + (2 - D)}$	$\frac{2nV_o}{n(3D + 2) + (2 - D)}$
[24]	1/1/1/6/5	$\frac{2 + n + nD}{(1 - D)^2}$	$\frac{V_o}{2 + n + nD}$	$\frac{(1 + n)V_o}{2 + n + nD}$
Proposed converter	1/1/1/6/5	$\frac{2 + 2n - nD}{(1 - D)^2}$	$\frac{V_o}{2 + 2n - nD}$	$\frac{(1 + n)V_o}{2 + 2n - nD}$

#Note: S = Switch, L = Inductor, CL = Coupled Inductor, D = Diode, C = Capacitor

Figure 5 depicts the graph of the voltage gain against the duty cycle of the proposed converter and the converters presented in [23] and [24] operating at identical conditions: CCM and $n = 2$. The proposed converter offers a larger voltage conversion ratio for duty ratios less than 0.66 when compared to the converter in [23]. The voltage gain of the proposed converter is greater than that of the converter in [24] so far as the duty cycle is less than 0.5. As a result, the voltage gain of the proposed converter is larger than that of the converters in [23] and [24], particularly at lower duty ratios. Thus, the proposed converter uses same turns ratio but smaller duty ratio to achieve the desired voltage gain decreasing the conduction loss and increasing conversion efficiency.

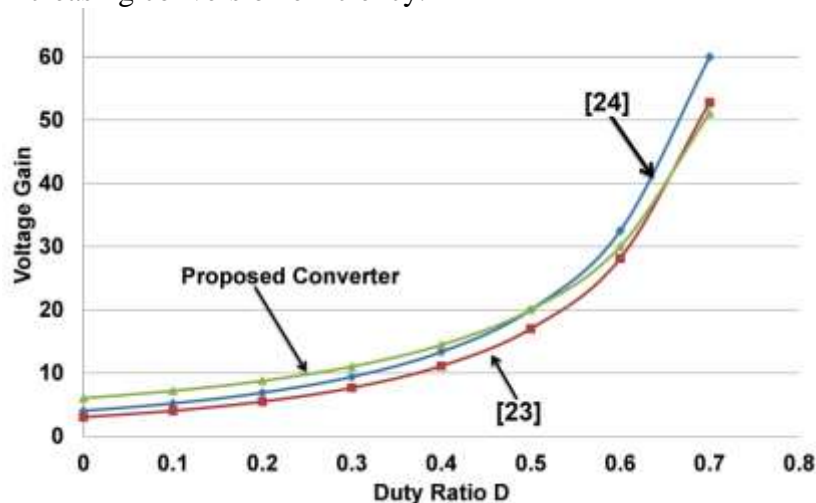


Fig. 5: Comparison of voltage gain

Voltage stresses on switches of these converters, normalized by the output voltage V_o , at duty ratio $D = 0.45$ are compared and presented in Fig. 6. The proposed converter's switch is subject to lower voltage stress than the converters presented in [23] and [24] that allows building the proposed converter with low-power MOSFETs having low R_{DS_ON} , which increases efficiency and reduces cost.

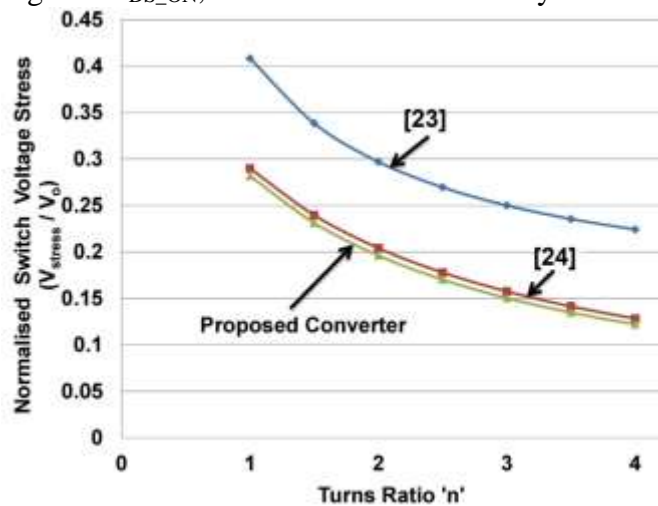


Fig. 6: Comparison of voltage stress on switch

4 - Results and discussion

PSpice software is used for simulation to evaluate the working principle and validate performance of the proposed converter. Figure 7 depicts the simulation circuit diagram.

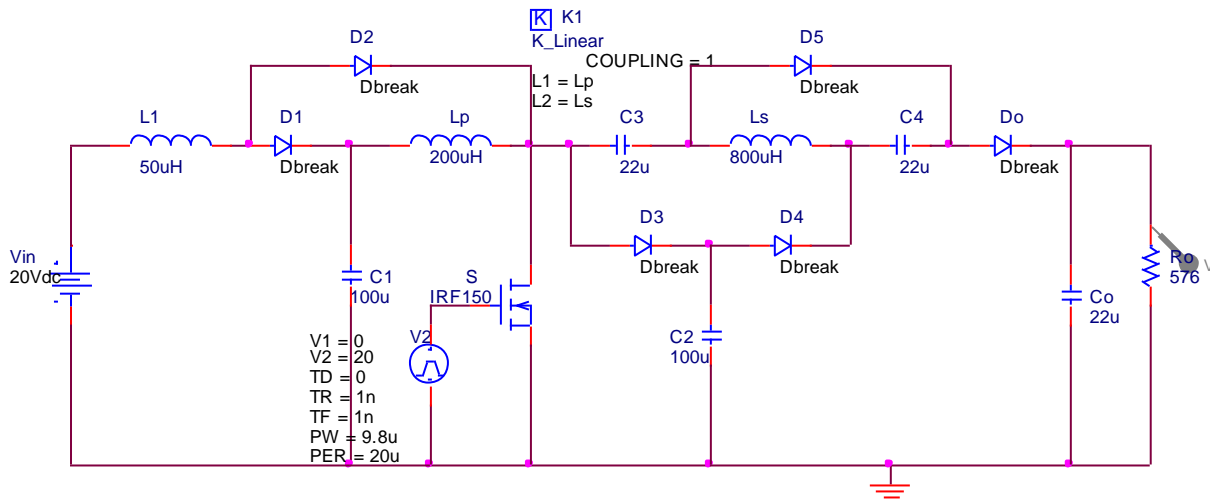


Fig. 7: PSpice simulation circuit diagram of the proposed converter

The circuit component values are calculated for output voltage of 380V, input voltage of 20V at 250W output power. The component values selected for simulation along with duty ratio and turns ratio are given in Table 2.

Table 2 Component values used for Simulation

V_{in}	Input Voltage	20V
V_{out}	Output Voltage	380V
P_o	Output Power	250W
f_s	Switching frequency	50 kHz
L_1	Inductor	50 μ H
L_m	Magnetizing inductor	200 μ H

n	Turns ratio = N_s/N_p	2
D	Duty ratio	0.49
C_1 and C_2	Capacitors	100 μ F
C_3 , C_4 and C_0	Capacitors	22 μ F
R_o	Load resistor	576 Ω

Typical simulated waveforms are shown in Fig. 8 and a summary of results are presented in Table 3.

Table 3 Summary of simulation result

Parameter	V_{in}	V_o	$V_{SW(OFF)}$	$V_{DO(OFF)}$	$V_{D1(OFF)}$	$V_{D2(OFF)}$	$V_{D3(OFF)}$	$V_{D4(OFF)}$	$V_{D5(OFF)}$
Simulation Result	20V	336.1V	68.5V	201V	32V	32V	67V	201V	134V

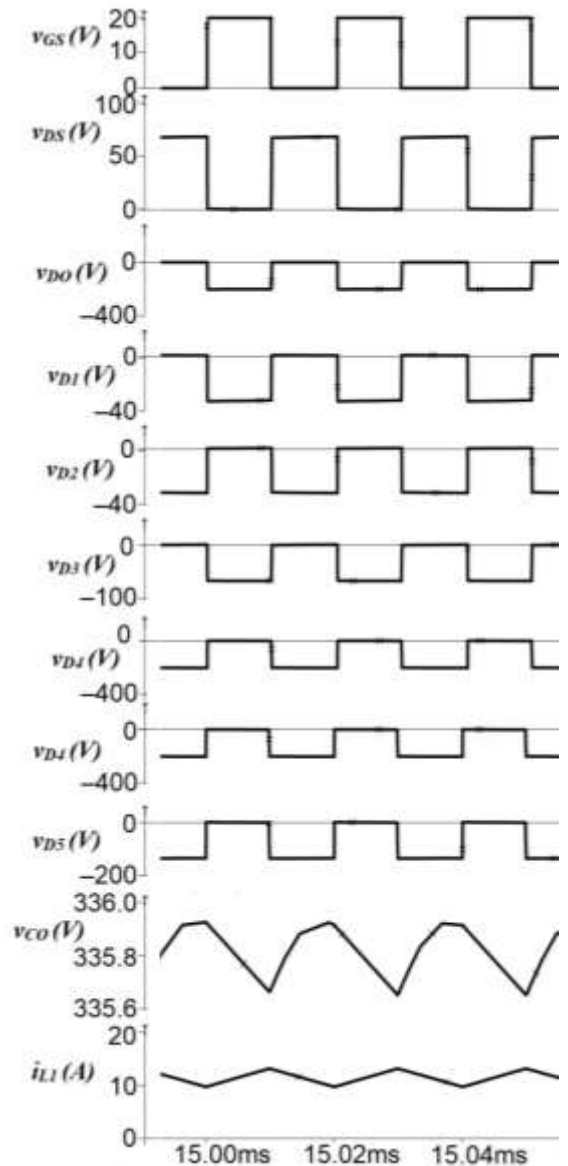


Fig. 8: Typical simulated waveforms of the proposed converter

The simulation results demonstrate that the switch voltage stress is 68.5V this being very small and around 20% of the output voltage which permits utilization of low power rated MOSFET having low on-

resistance as a switch which results in reduction in conduction loss and cost. Due to the very small voltage stresses on D_1 , D_2 as well as D_3 , low forward voltage drop diodes may be utilized to reduce power losses of diodes. It also helps in reducing diode's reverse recovery problem. The high voltage conversion ratio of 17 at lower turns ratio of 2 at low duty ratio D of 0.49 with low switch voltage stress of 68.5V is result of the appropriate placement of diodes and capacitors with the coupled inductor's secondary to form VMC. It is also clear from Fig. 8 that the proposed converter's input current of is continuous and has low ripple. This is important feature for the converter used in FC based applications because continuous low ripple input current improves FC stack performance.

5 – Conclusion

A high voltage gain dc-dc converter which combines a coupled inductor quadratic boost converter with an integrated VMC is presented in this paper. The appropriate placement of diodes and capacitors with the coupled inductor's secondary to form the VMC yields a high voltage gain of 17 at the turns ratio n of 2 and the duty cycle D of 0.49. As a result, the proposed converter obtains very high voltage gain at small duty ratio and small turns ratio. The switch voltage stress is considerably decreased and is around 20% of the output voltage. Thus a low power rated and low on-resistance MOSFET may be utilized as a switch for enhancing the efficiency with reduction in the cost of the converter. The coupled inductor's leakage energy has been recycled resulting in improved conversion efficiency. In the proposed topology, an inductor is directly connected to input voltage source hence the input current exhibits low ripple. These desirable characteristics make the proposed converter an attractive candidate for the front-end converters for use in sustainable energy systems especially with FC applications.

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